

## AMALIA PLATFORM: DESIGN ENABLER

### Revolutionize design centering

**Design Enabler (DE)** accelerates design-centering and in doing so helps in optimizing the utilization of experienced engineers.

After the porting of schematics, the design in target technology may fail to meet some of the performance parameters. DE employs Thalia-developed AI algorithms to identify *Key Devices* impacting the circuit performance and guides the designer in the direction to adjust them.

## Accelerate design centering

### AI helps optimize resource loading

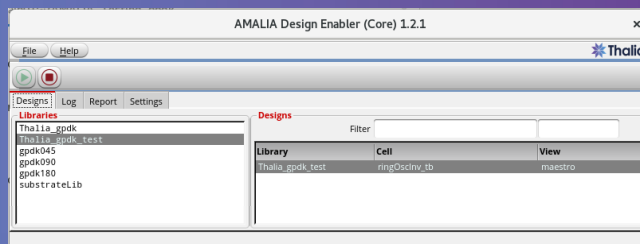
AI assistance provides automation with intelligence, reducing the reliance on the most experienced engineers freeing them for other critical tasks

### Reduces time for design-centering phase

Pinpoints root-cause devices leading to performance issues

### Designer-in-the-Loop

Acting as a design assistant, Design Enabler empowers the designer to leverage automation and built-in intelligence to quickly achieve design constraints



Key device recognition  
Library : ota circuit  
Cell : ota\_tb  
Maestro : maestro ac

Pinpointing devices with greatest impact on parameters

Impacts for Combined corner									
Instances	Cell	Type	Parameter	phaseMargin	unityGainFreq	gainDCV	gainDCV75		
Pb2b Pb4b Pb5b Pb1b Pb6b	ota_bias	pmos	fw	+13.1					
Pb2b Pb4b Pb5b Pb1b Pb6b	ota_bias	pmos	l	+11.5	-11.3	+35.2	+35.4		
Ntail	ota	nmos	fw	-12.5	+31.4	+12.7	+14.3		
Ntail	ota	nmos	l	+11.5	-17.0	-16.3	-17.0		
Cloud1 Cloud2	ota_tb	cpin	c	+10.2	-34.4	0.0	0.0		
P3b P3c P3d P4b P4c P4d	ota	pmos	fw	-10.2	+10.4	+11.7	+16.5		
P3b P3c P3d P4b P4c P4d	ota	pmos	l	(T)0.1	+0.4	-11.5	-15.2		
P2c P1c	ota	pmos	fw	-10.3	-10.4	+10.1	+5.2		
P2c P1c	ota	pmos	l	-12.5	+11.3	+10.1	-11.7		
Ntailc	ota	nmos	fw	-10.1	+11.1	+10.5	+10.6		
Ntailc	ota	nmos	l	+10.1	-10.7	-10.3	-10.3		
M1 M0 MN6 MN4 MN5	ota_bias	pmos	l	0.0	0.0	0.0	0.0		
M1 M0 MN6 MN4 MN5	ota_bias	pmos	fw	0.0	0.0	0.0	0.0		

## Key Features

### Maestro models

Manage multiple Maestro simulations in Cadence® simulation environment

### Tabulated performance reports

Comprehensive report of all device parameters identifying where performance is impacted

### Devices matching & scaling

Mirrors a human approach to Analog design aided by AI to speed up design centering

### Color coding for direction of impact

Easy visual indication to identify where improvements are required and the direction

### Consistent platform-based-GUI

Familiar, intuitive interface to reduce learning curves and increase productivity

### Interactive set up with EDA industry solutions

Cadence Virtuoso®

Siemens EDA Analog FastSPICE Platform

### Trademark acknowledgment

Cadence and Virtuoso are Marks of Cadence Design Systems

Use of these names and other company's and products does not imply endorsement.



## The AMALIA difference

AMALIA Platform is an advanced, comprehensive IP reuse solution.

Leveraging automation and AI/ML capabilities, it drastically reduces the complexity, cost and time traditionally associated with migrating and enhancing existing analog, mixed-signal and RF design IPs.

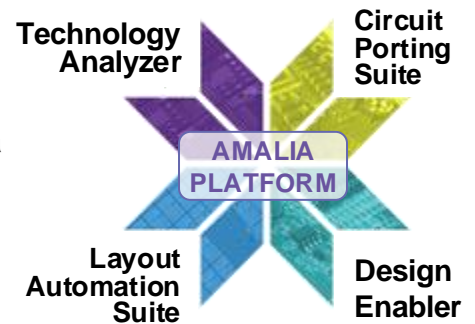
Four functional solutions provide a powerful portfolio to successfully accelerate analog reuse.

## Navigating the design migration challenge

Migrating an IC or IP to a different process technology or node unlocks new revenue opportunities, enhancing performance and secure a reliable second source supply.

However, design migration is a conundrum for semiconductor business leaders. While it opens new business opportunities, analog and mixed-signal migrations are expensive and fraught with risks.

AMALIA Platform addresses this challenge by providing a proven, unique end-to-end solution which reduces the engineering effort from man-months to man-weeks, reducing costs while significantly mitigating risks.



## Contact us today

Contact our sales team today to discuss how AMALIA can accelerate your next design migration

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